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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,247	09/24/2003	Mitsuaki Osame	0756-7202	2065

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ERIC ROBINSON.
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
TAN, VIBOL	
ART UNIT	PAPER NUMBER
2819	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/668,247	OSAME ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,6,8,10-32 and 34* is/are allowed.

6)☒ Claim(s) *7,9,33,35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Further consideration of this instant application leads to new ground of rejection; as a result, the finality of the last office action is withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 7, 9, 33 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Osame (US 2003/0210219 A1).

The applied reference has a common assignee or inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In claim 7, Osame teaches all claimed features in Fig. 4, a clocked inverter comprising: first to third transistors (101, 201, 202) connected in series, and a fourth transistor and a fifth transistor (105, 103) connected in series, wherein: gates of the

fourth transistor (105) and the fifth transistor (103) are connected to each other (at LAT); drains of the fourth transistor and the fifth transistor are each connected to a gate of the first transistor solid node on the gate of 101); sources of the first transistor (101) and the fifth transistor (103) are each electrically connected to a first power (VDD); sources of the third transistor (202) is electrically connected to a second power source (VSS via 102); and an amplitude of a signal inputted (DATA) to a source of the fourth transistor is smaller ([0048], High potential of data signal is 6V) than a potential difference between the first power source and the second power source; the first power source is a high potential power source (9V, [0048]); the second power source is a low potential power source (VSS is 0V); the first transistor (101), the second transistor (201), and the fifth transistor (103) are each a P-type transistor; and the third transistor (202) and the fourth transistor (105) are each an N-type transistor.

In claim 9, Osame teaches all claimed features in Fig. 4, a clocked inverter comprising: first to third transistors (102, 202, 201) connected in series, and a fourth transistor and a fifth transistor (106, 104) connected in series, wherein: gates of the fourth transistor (106) and the fifth transistor (104) are connected to each other (at LATB); drains of the fourth transistor and the fifth transistor are each connected to a gate of the first transistor solid node on the gate of 102); sources of the first transistor (102) and the fifth transistor (104) are each electrically connected to a first power (VSS); sources of the third transistor (201) is electrically connected to a second power source (VDD via 101); and an amplitude of a signal inputted (DATA) to a source of the fourth transistor is smaller ([0048], High potential of data signal is 6V) than a potential

difference between the first power source and the second power source; the first power source is a low potential power source (VSS is 0V); the second power source is a high potential power source (VDD is 9V); the first transistor (102), the second transistor (202), and the fifth transistor (104) are each an N- type transistor; and the third transistor (201) and the fourth transistor (104) are each a P-type transistor.

In claim 33, Osame further teaches clocked inverter according to claim 7, wherein the fourth transistor is replaced with an analog switch ([0029] and [0031]).

In claim 35, Osame further teaches clocked inverter according to claim 9, wherein the fourth transistor is replaced with an analog switch ([0029] and [0031]).

4. Claims 1-4, 6, 8, 10-32 and 34 appear to comprise allowable subject matter(s).

Response to Arguments

5. In view of further consideration, new ground(s) of rejection have been set forth in detailed above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VIBOL TAN
PRIMARY EXAMINER